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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 5

Application Number	72804
Filing Date	January 11, 2002
First Named Inventor	Chason et al.
Art Unit	2811
Examiner Name	Jones, J.
Attorney Docket	72804

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
JMD		US-6,395,124	5/28/02	Oxman et al.	
JMD		US-6,276,278	4/23/02	Egawa et al.	
JMD		US-6,352,881	3/5/02	Nguyen et al.	
JMD		US-6,352,878	3/5/02	Mostafazadeh et al.	
JMD		US-6,335,571	1/01/02	Capote et al.	
JMD		US-6,341,418	1/29/02	Brouillette et al.	
JMD		US-6,323,062	11/27/01	Gilleo et al.	
JMD		US-6,297,560	10/2/01	Capote et al.	
JMD		US-6,287,893	9/11/01	Elenius et al.	
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JMD		US-6,194,788	2/27/01	Gilleo et al.	
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JMD		US-6,168,972	1/02/01	Wang et al.	

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[6]
JMD		WO 99/03597	1/28/99			
JMD		WO 99/04430	1/28/00			
JMD		WO 99/56312	11/4/99			
JMD		WO 00/54322	9/14/00			
JMD		WO 01/20658 A1	3/22/01			

Examiner Signature		Date Considered	10/22/02

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JMJ		US-6,132,656	10/17/00	Zhou et al.	
JMJ		US-6,121,689	9/19/00	capote et al.	
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JMJ		US-6,017,634	1/25/00	Capote et al.	
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JMJ		US-5,128,746	7/7/92	Pennisi et al.	
JMJ		US-2001/0012580 A1	8/9/01	Cobbley et al.	
JMJ		US-2002/0014703 A1	2/7/02	Capote et al.	
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Examiner Signature	Jennifer M Blum	Date Considered	10/22/02

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Application Number	72804
Filing Date	January 11, 2002
First Named Inventor	Chason et al.
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
JMJ		Robert V. Burress et al., *"A Practical, Flip-Chip, Multi-layer Pre-Encapsulation Technology for Wafer-Scale Unterfill,"* IEEE, 5 pages (2001)	
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JMJ		Jicun Lu et al., *"Solder Wetting in a Wafer-Level Flip Chip Assembly,"* IEEE, 6 pages (2001)	
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JMJ		Larry Crane et al., *"Development of Wafer Scale Applied Reworkable Fluxing Underfill for Direct Chip Attach, Part II,"* APEX, pg. 1-6, (2002)	
JMJ		Jing Qi et al., *"Assembly of Flip Chips Utilizing Wafer Applied Underfill,"* APEX, 7 pages (2002)	

Examiner Signature	Jennifer M Jones	Date Considered	10/28/02

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
JMN		Dr. Larry Crane et al., *"Making Direct Chip Attach Transparent to Surface Mount Technology,"* Chip Scale Review pg. 50-53 (1999)	
JMN		Mr. Albert Capote et al., *"A Novel Flip-Scale package Using Pre-Applied Multilayer Flip-Chip Under-Encapsulation,"* Pan Pacific Microelectronics Symposium pg. 153-158 (1999)	
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JMN		C. Quentin, et al. *"Wafer Level Application of Reworkable Underfill,"* IMAPS, pg. 284-292 (1999)	
JMN		Dr. Ken Gilleo et al. *"Wafer-Level Flip Chip Enabled with Solid Underfill,"* HD International Conference, pg. 128-133 (2000)	
JMN		L. Nguyen et al., *"Solder Joint Shape Formation Under Constrained Boundaries in Wafer Level Underfill,"* IEEE, 6 pages (2000)	
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Examiner Signature		Date Considered	10/22/02

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JMD		Wayne Johnson, Ph.D. et al., *"Wafer Applied Underfills for Flip Chip Assembly,"* ICAPS, 11 pages (2002)	
JMD		Q. Tong et al., *"Novel Materials and Processes for Wafer Pre-Apply Flip Chip and Chip Scale Packaging,"* IEEE, 6 pages (2002)	
JMD		Q. Tong et al., *"Encapsulant Materials and Processes for Wafer Level-Chip Scale Packaging (WL-CSP),"* IEEE, 7 pages (2002)	
JMD		Robert V. Burress et al., *"A Novel, Wafer-Scale Technology for Addressing Process and Cost Obstacles Associated with Unterfilling FCOB,"* IEEE, 4 pages (2002)	

Examiner Signature	Jennifer M Dolan	Date Considered	10/22/02

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